

**CSEE 4280: Lab 2: Design, Simulating & Implementing a 4-Bit ALU**

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**Contributions:**

• Pre-lab design and analysis:

Habilou - 50% Kingsley - 50%

• In-lab module and testbench design

Habilou - 50% Kingsley - 50%

• In-lab testbench simulation and analysis

Habilou - 50% Kingsley - 50%

• In-lab FPGA synthesis and analysis

Habilou - 50% Kingsley - 50%

• Lab report writing

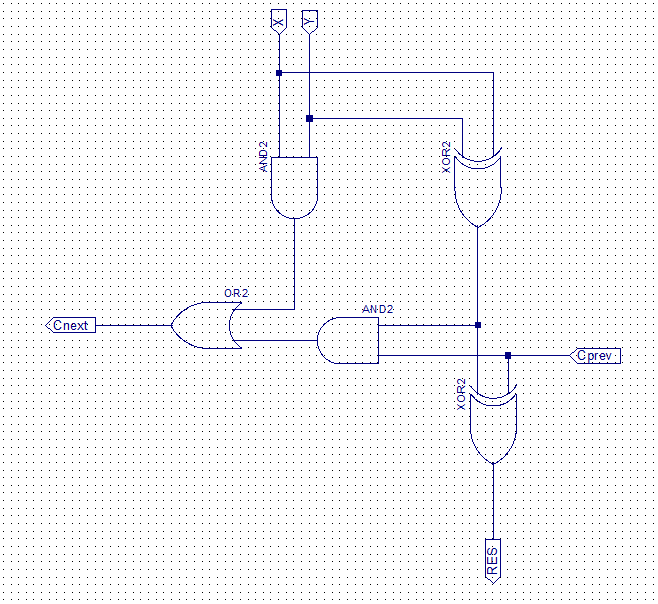
Habilou - 50% Kingsley - 50%

1. **Preface**

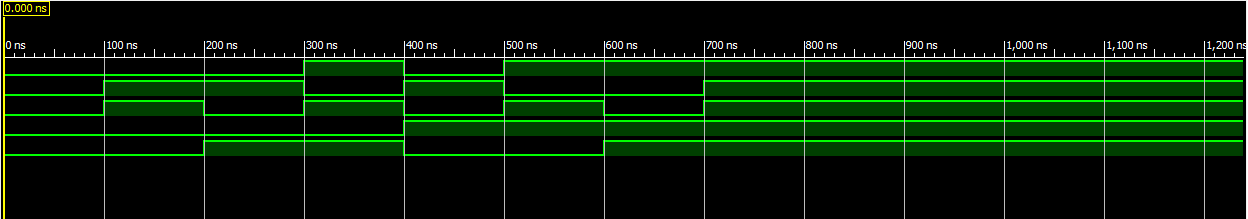
In this lab we designed an 8-bit arithmetic logic unit that could perform addition and subtraction operations. After that we design a second 4-bit arithmetic logic unit that performs four logic operations and 4 arithmetic operations. Both the 8-bit and the 4-bit ALUs build upon the full-adder. In order to perform all 8 operations we then need to design two devices that will connect to the full-adder’s inputs: a logic extender and an arithmetic extender.

We will then put all of these elements together with a binary-to-seven-segment module that we will also design. Our finished ALU will have two 4-bit inputs, two outputs, and three control signals (which control which operation to perform.

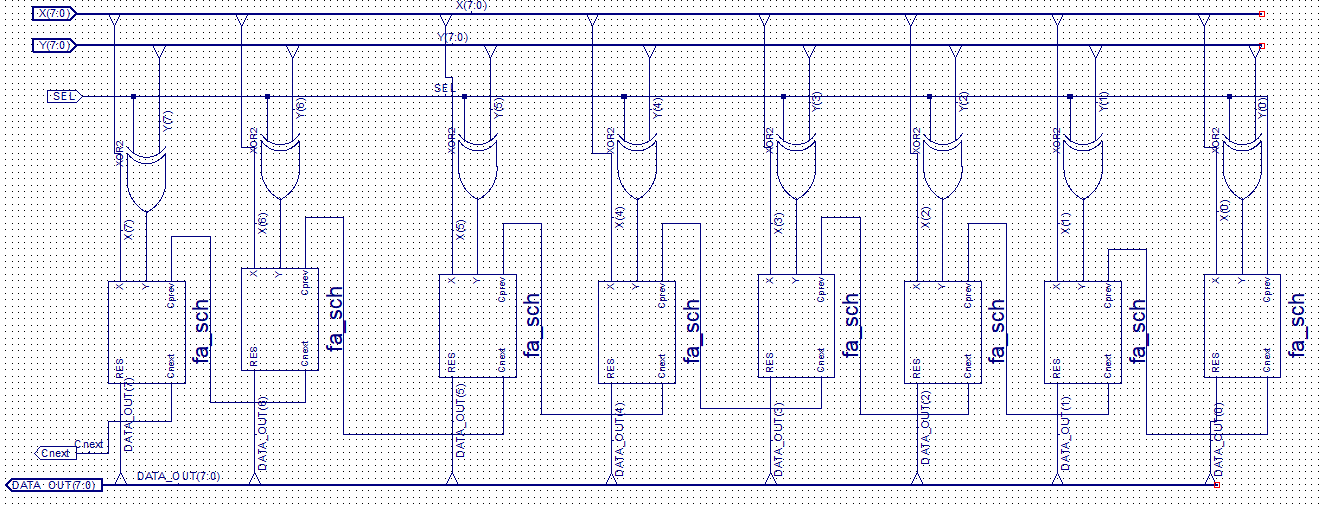
1. **Implementation Details**
   1. **Simplified ALU Component**

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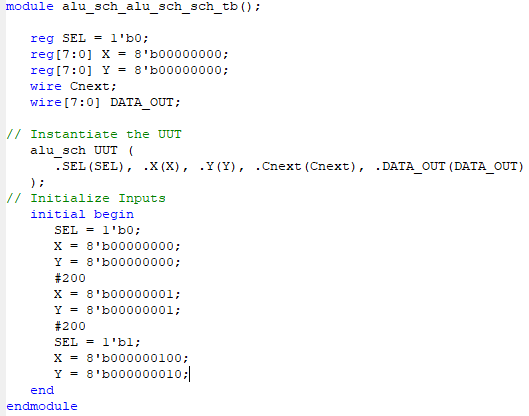
**Full Adder Schematic**

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**Full Adder Waveform**

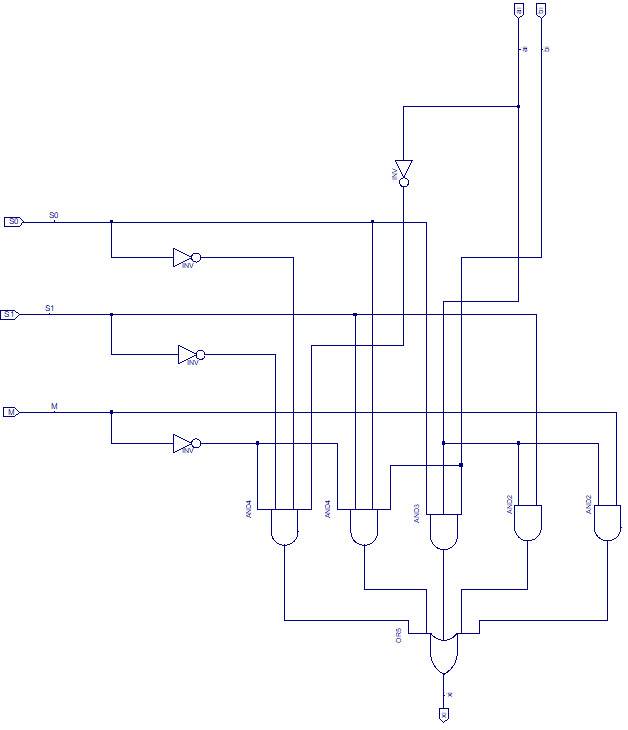
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**ALU Schematic**

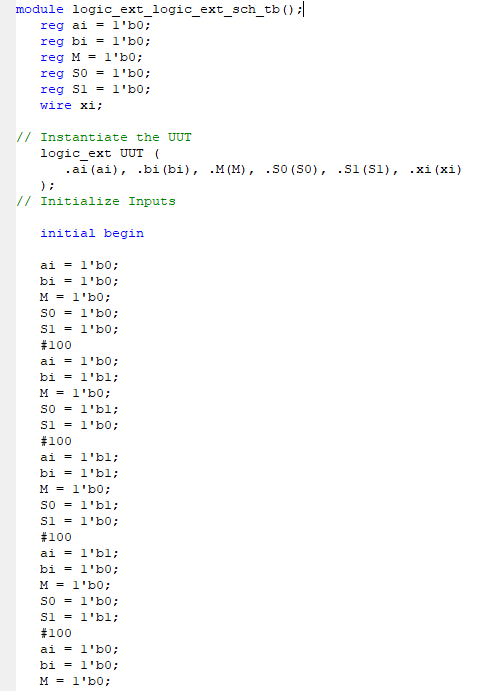
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**ALU Testbench**

* 1. **Logic Extender Component**

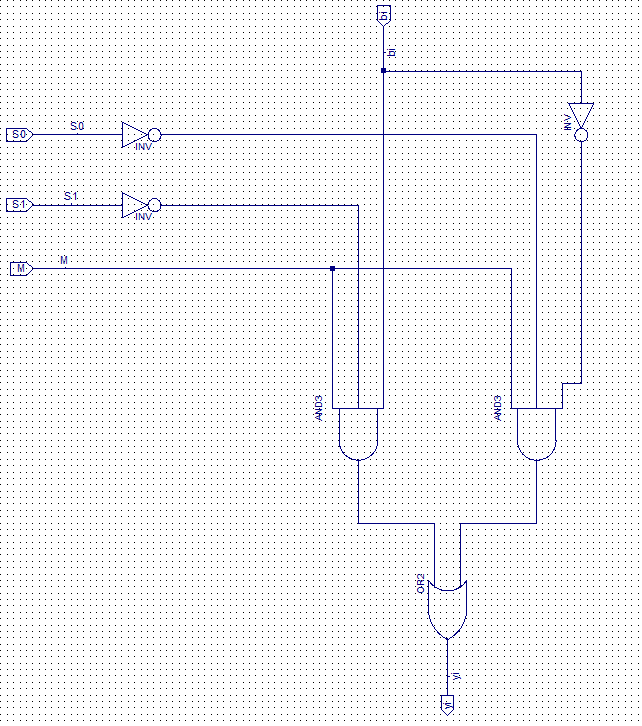
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**Logic Extender Schematic**

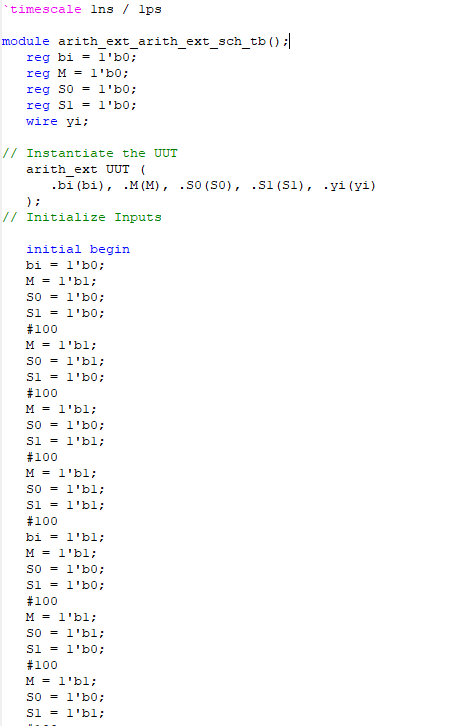
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**Logic Extender Testbench**

* 1. **Arithmetic Extender**

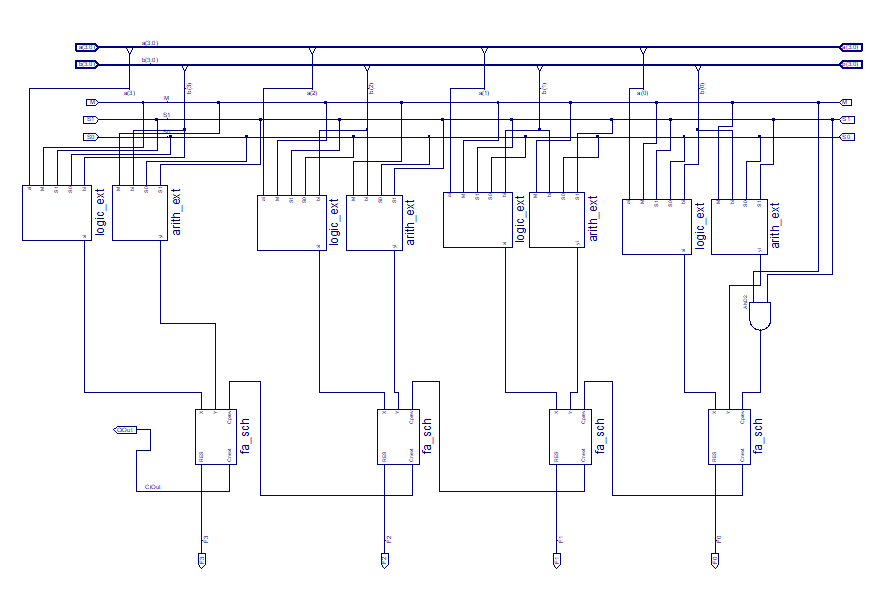
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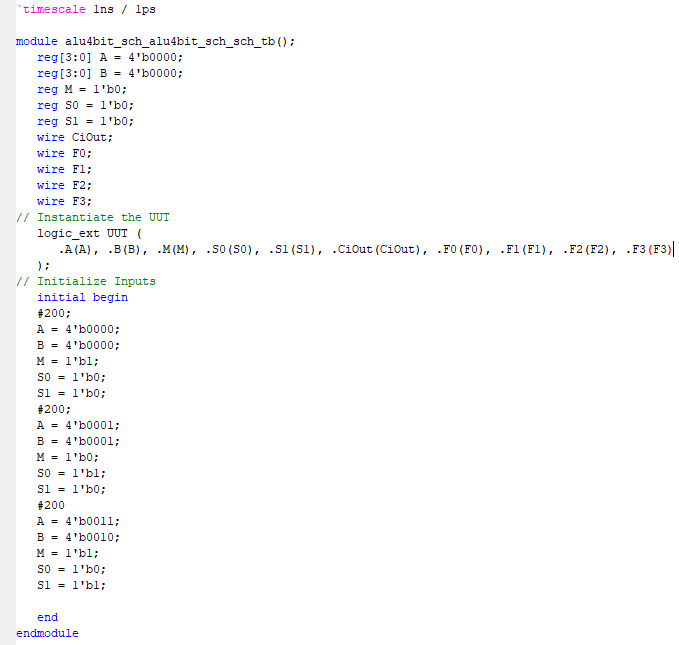
**Arithmetic Extender schematic**

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**Arithmetic Extender Testbench**

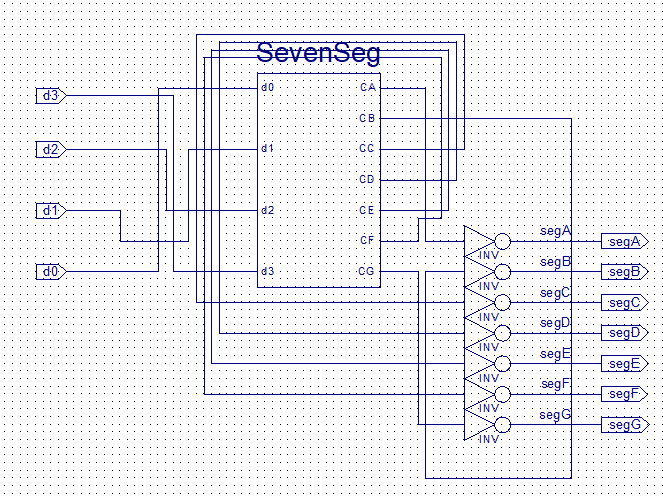
**4-Bit ALU Component**

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**4-Bit ALU Schematic  
  
  
  
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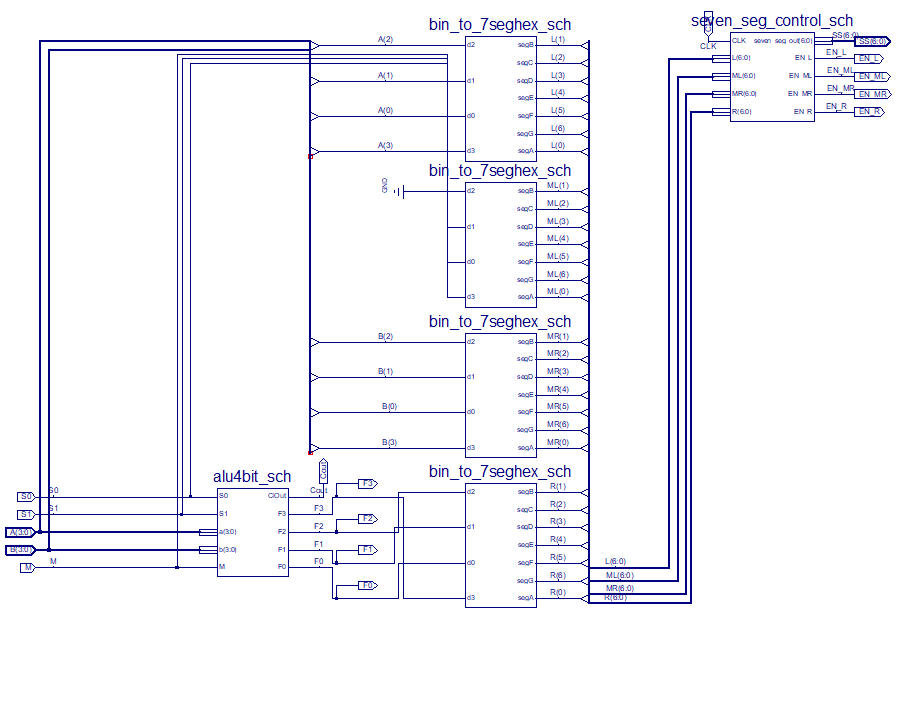
**4-Bit ALU Testbench**

* 1. **4-Bit to 7-segment Converter**

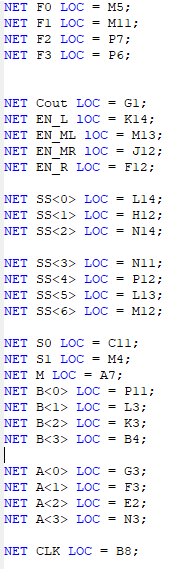
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**4-Bit to 7-Seg Schematic**

* 1. **Everything Comes together**

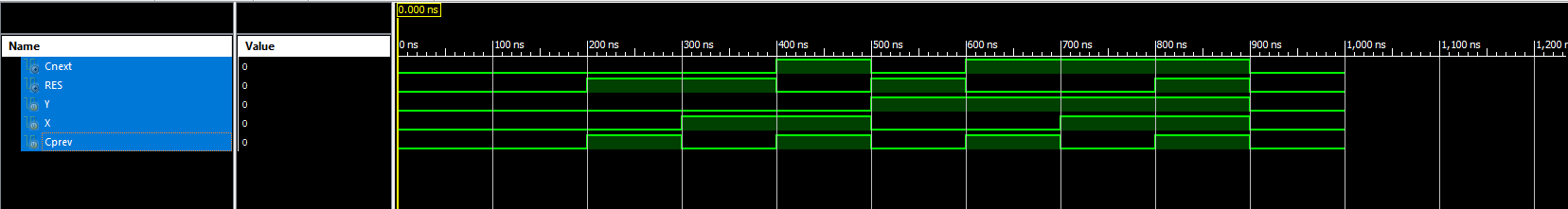
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**4-Bit ALU Board Schematic**

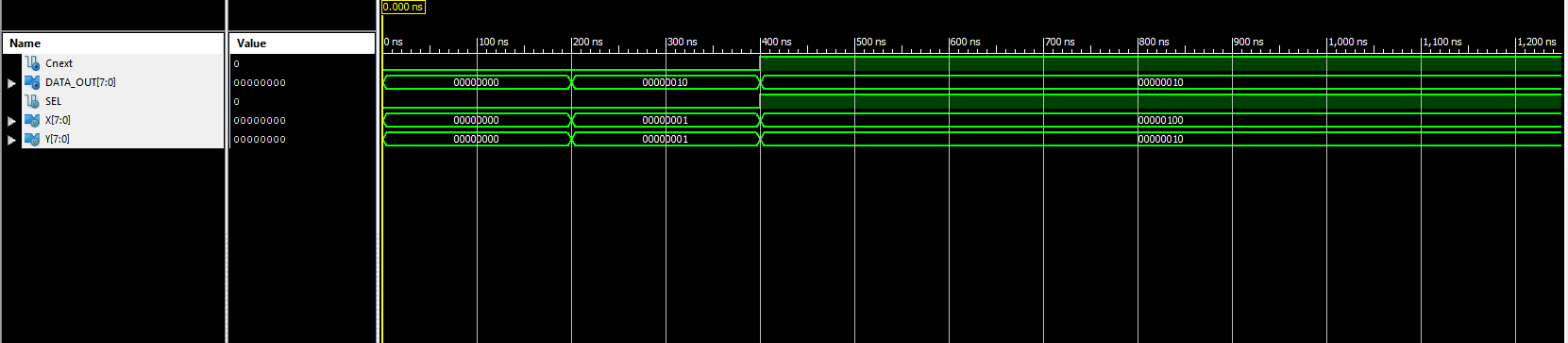
* 1. **UCF File**

1. **Experimental Results**

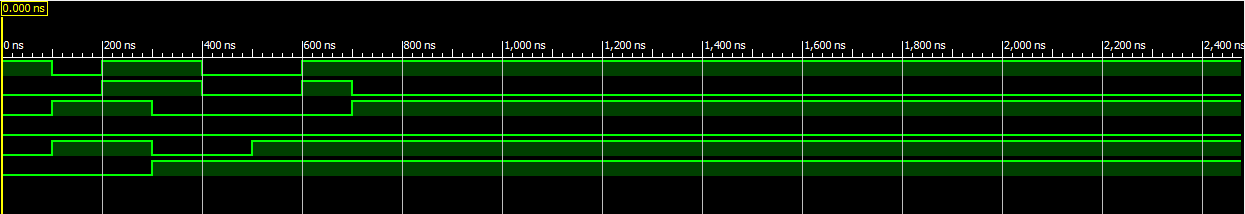
* 1. **Full Adder**

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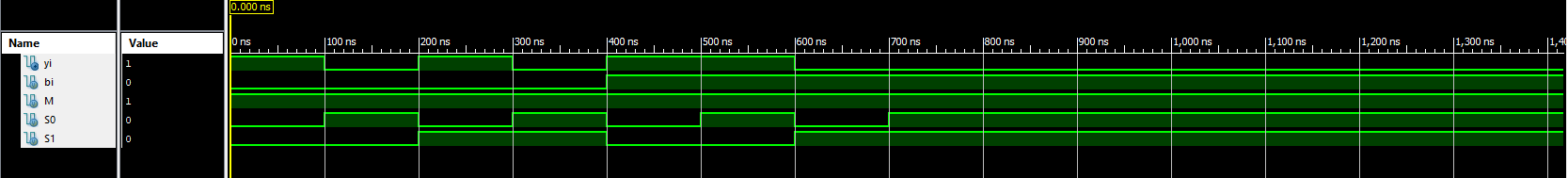
**This waveform confirms the functionality of our ALU schematic because we were able to test our result against the table given in page 3**

* 1. **ALU Component**

**This waveform confirms the functionality of our schematic because we were able to performs different operations on our inputs and the result obtained from this waveform confirmed our predictions**

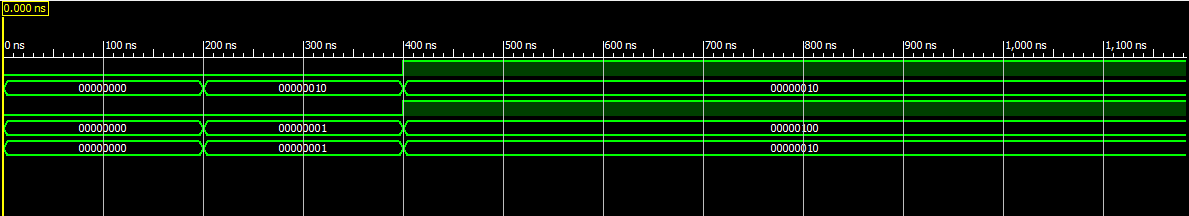
* 1. **Logic Extender Component**

**This waveform confirms the functionality of our schematic because by using signal M, we are able to control whether the logic extender should be utilized or bypassed. The signals S0 & S1 determines which operation to perform on the inputs A & B.**

* 1. **Arithmetic Extender**

**This waveform confirms the functionality of our arithmetic schematic because we were able to perform all the functions (Decrement, add, subtract & increment) on different input value.**

* 1. **4-Bit ALU Component**

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**This waveform confirms that our schematic works as intended because we were able to perform each operation by changing the value of M, S1 & S0 and the result we obtain from the waveform.**

1. **Conclusion**

**In conclusion, we were able to build all the components required from this lab, we were also able to test the functionality of each component and finally, we were able to demo our final work to the Tas.**